



1 8. The method of claim 1, wherein the amorphous semiconductor layer <sup>ob; mch</sup>  
2 includes silicon germanium.

1 9. The method of claim 7, wherein the amorphous semiconductor layer  
2 includes silicon germanium.

1 10. The method of claim 9, wherein the annealing step takes place at a  
2 temperature sufficient to melt the amorphous semiconductor layer and is below the  
3 melting temperature of the substrate.

1 11. The method of claim 10, wherein the annealing step is performed by  
2 an excimer laser.

3 12. A method of manufacturing an ultra-large scale integrated circuit  
4 including a transistor, the method comprising steps of:  
5 depositing an amorphous silicon germanium material above a top  
6 surface of a semiconductor substrate;  
7 annealing the amorphous silicon germanium material;  
8 depositing an amorphous silicon material above the silicon  
9 germanium material;  
10 annealing the amorphous silicon material; and  
11 providing a source region and a drain region for the transistor, the  
12 source region and the drain region being deeper than a combined thickness of the  
13 silicon germanium material and the silicon material.

1 13. The method of claim 12, further comprising:  
2 providing a gate structure before providing a source region and a  
3 drain region step.

1 14. The method of claim 12, further comprising:  
2 providing an oxide layer over the silicon material after the second  
3 annealing step.

1           15.    The method of claim 12, wherein the silicon germanium material is a  
2   single crystalline layer after the first annealing step.

1           16.    The method of claim 12, wherein the silicon material is a single  
2   crystalline layer after the second annealing step.

1           17.    The method of claim 12, wherein the silicon material is 100-150Å  
2   thick.

1           18.    The method of claim 12, wherein the annealing temperature for the  
2   first and second annealing steps is at or above 1100°C and below 1400°C.

1           19.    A process of forming a transistor with a silicon germanium channel  
2   region, the process comprising:  
3                    depositing a thin amorphous silicon germanium material above a top  
4   surface of a semiconductor substrate;  
5                    annealing the silicon germanium material to form single crystalline  
6   silicon germanium material;  
7                    depositing a thin amorphous silicon material above the single  
8   crystalline silicon germanium material;  
9                    annealing the silicon material to form single crystalline silicon  
10   material; and  
11                   providing a source region and a drain region for the transistor, the  
12   source region and the drain region extending into the substrate.

1           20.    The process of claim 19, wherein the silicon germanium material is  
2   200-500Å thick.

1           21.    The process of claim 20, wherein the silicon material is 100-150Å  
2   thick.

1           22.    The process of claim 19, wherein the annealing steps are excimer  
2   laser annealing steps.

1           23.     The process of claim 22, wherein the excimer laser annealing steps  
2     use a wavelength of 308 nanometers.

1           24.     The process of claim 23, the source and drain regions each including  
2     an extension.

1           25.     A transistor comprising a source and drain region and a channel  
2     region, the source and drain regions being at least partially disposed in a bulk  
3     semiconductor substrate, the channel region being disposed between the source and  
4     drain regions, the channel region including a silicon germanium layer and a silicon  
5     cap layer.

1           26.     The transistor of claim 21, wherein the source and drain regions are  
2     silicided to eliminate any effect of germanium in the source and drain regions.

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